REMARKS

Claims 1, 3-12, 14-19, and 21-24 remain pending in the application.

35 U.S.C. § 102 Rejection:

Claims 19, 21-22 and 24 were rejected under 35 U.S.C. § 102(e) as being anticipated by Rhee, U.S. Patent 6,804,790. Applicant respectfully traverses this rejection.

Rhee fails to teach or suggest all of the elements of claim 19. Rhee teaches a multi-processor computing system including a plurality of processing units in which each of the plurality of processing units operates at clock frequency and a coordinating protocol is used to assign tasks and operations to any of the plurality of processing units in a manner such that the power efficiency of the system is optimized.

Independent claim 19 recites:

> "An apparatus for start-up of a computer system comprising a plurality of computing units, the apparatus comprising means for setting a different clock frequency for each unit so that said units each operate at a different frequency, each frequency differing from another frequency by at least a predetermined minimum **bandwidth**, and **means for determining** said predetermined minimum **bandwidth** as a **multiple** of a predetermined **base frequency**" (Emphasis added).

In the office action, the Examiner contends that Rhee teaches a "means for determining said predetermined minimum bandwidth as a multiple of a predetermined base frequency" in Fig. 1, col. 2 lines 17-21 and 48-49, col. 3, lines 28-31 and 51-62, col. 4 lines 30-32 and col. 6 lines 3-7. Fig. 1 of Rhee illustrates a block diagram of a plurality of processors operating at clock speeds f_1-f_n. The portions of the Rhee's specification cited by the Examiner state the following:

"In a preferred embodiment, the first and second processing units are interconnected. The first processing unit operates at a first clock frequency, and the second processing unit operates at a second clock frequency. The first clock frequency may be lower than the second clock frequency." (Rhee, col. 2, lines 17-21).

"In a preferred embodiment, each of the plurality of processing units operates at a different clock frequency." (Rhee, col. 2, lines 48-49).

"In a preferred embodiment, the first processing unit operates at a clock frequency of 32 kHz and the second processing unit operates at a clock frequency of 4 MHz. The power source may be a battery." (Rhee, col. 3, lines 28-31).

"Networked processing system 10, FIG. 1, includes a number of interconnected processing units 12, 14, 16, 18, and 20. There should be at least two interconnected processing units, and there may be any number N of these processing units in system 10. Each processing unit operates at a given clock frequency, f_1, f_2, f_3, f_4, . . . f_N, respectively. The clock frequencies may all be the same, one or more of the clock frequencies may be the same, or all of the clock frequencies may be different. In a preferred embodiment, each processing unit operates at a different clock frequency, with $f_1 < f_2 < f_3 < f_4 < \ldots f_N$." (Rhee, col. 3, lines 51-62).

"As shown in FIG. 3, there are N processing units 50, 52, 54, each operating at a respective clock frequency of f_1, f_2, . . . f_N, with $f_1 < f_s < \ldots f_N$." (Rhee, col. 4, lines 30-32).

"Step 80 of providing a plurality of processing units, FIG. 4, includes providing at least first and second processing units. Each of the processing units operates at a clock frequency. In a preferred embodiment, the clock

frequencies of each of the plurality of processing units is different, although this is not a necessary limitation." (Rhee, col. 6 lines 3-7).

Each of the above citations from Rhee, which are used to support the Examiner's contention, teach a plurality of processing units, each operating at different clock frequencies. However, nowhere in these citations or elsewhere within Rhee is there any teaching or suggestion of any "means for **determining** said predetermined minimum **bandwidth** as a multiple of a predetermined base frequency" as recited in combination with the other features of claim 19. In fact, Rhee is silent with respect to any predetermined minimum bandwidth for which each frequency differs from another frequency, much less **determining** a minimum bandwidth for which each frequency differs from another frequency or any **means for determining** a minimum bandwidth for which each frequency differs from another.

For at least these reasons, Applicant submits that Rhee fails to teach or suggest all of the elements of independent claim 19 and its associated dependent claims. Accordingly, removal of the 35 U.S.C. § 102(a) rejection is respectfully requested.

35 U.S.C. § 103(a) Rejection:

Claims 1, 3-12, and 14-18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Rhee in view of Andrea, U.S. Patent 5,506,545. Applicant respectfully traverses this rejection.

The proposed modification would change the principle of operation of the Rhee reference, and would render it unsatisfactory for its intended purpose. Thus there is no suggestion to combine the references. Rhee is directed toward a system wherein power usage is minimized, while power efficiency is optimized:

"A multi-processor computing system included a plurality of processing units is provided in which each of the plurality of processing units operates at clock frequency and a coordinating protocol is used to assign

tasks and operations to any of the plurality of processing units in a manner such that the power efficiency of the system is optimized." (Rhee, Abstract).

This is further pointed out in the objects of the invention discussed in the summary of Rhee:

"It is therefore an object of this invention to provide a networked processing system in which power usage is minimized." (Rhee, col. 1, lines 58-60; emphasis added).

"It is a further object of this invention to provide a multi-tasking, multiple processor system in which the power efficiency is optimized." (Rhee, col. 1, lines 65-67, emphasis added).

In order to obtain these objectives, Rhee provides a coordinating protocol for coordinating usage of processing units such that the appropriate tasks are performed at the appropriate speeds:

"The invention results from the realization that, in a multi-tasking, multi-processor environment, the power efficiency of the system can be optimized by coordinating the usage of processing units such that tasks are run on the appropriate speed processing unit and unused processing units are placed in sleep mode.

This invention features a networked computing system with improved power consumption comprising a plurality of processing units including at least first and second processing units. A coordinating protocol is operative on the first and second processing units and controls the operation of the system such that the power consumption of the system is minimized." (Rhee, col. 2, lines 5-16; emphasis added).

In light of the above citations, Applicant submits that it is clear the apparatus taught by Rhee assigns clock frequencies to processing units on the basis of optimizing power efficiency and minimizing power consumption. In contrast, the system taught by Andrea produces a clock signal that **randomly** varies in frequency:

> "A spread-spectrum clock circuit is applied to microprocessor or other clocked digital electronic equipment for the purpose of reducing spectral emissions residing at harmonic and subharmonic multiples of the clock frequency. This clock randomly varies the frequency of its output within a frequency constraint bound centered at the average clock frequency." (Andrea, abstract; Emphasis added).

This is further illustrated by the apparatus shown in Andrea's Fig. 1, wherein the frequency of a clock signal is modulated by a random noise generating means. **Thus the proposed modification would change the principle of Rhee from one of assigning tasks to be run on an appropriate speed processing unit (in accordance with the coordinating protocol) to one wherein the operating speed of each processing unit varies with the random noise generating means of an associated clock circuit.** Furthermore **modifying Rhee with the clock circuit of Andrea, which provides a clock signal that randomly varies in frequency, would render Rhee unsatisfactory for its intended purpose of minimizing power usage and optimizing power efficiency,** as noted in the stated objects in Rhee.

MPEP 2143.01(V) states that "[if the] proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification." Applicant submits **that the proposed modification renders Rhee unsatisfactory for its intended purpose(s) of minimizing power usage and optimizing power efficiency.**

MPEP 2143.01(VI) states that "[if] the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being

modified, then the teachings of the references are not sufficient to render the claims prima facie obvious." Applicant submits that **the proposed modification would change Rhee's principle of coordinating the usage of processing units such that tasks are run on the appropriate speed processing unit** to one **wherein tasks are run on processing units with clock speeds having randomly varying frequencies.**

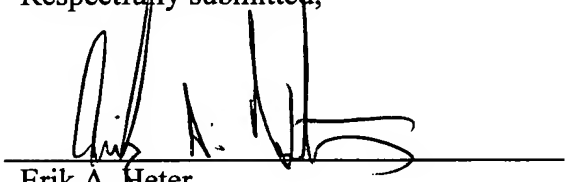
For at least these reasons, Applicant submits that there is no suggestion to combine the references. Accordingly, removal of the 35 U.S.C. § 103(a) rejection is respectfully requested.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5681-92600/EAH.

Respectfully submitted,



Erik A. Heter
Reg. No. 50,652
AGENT FOR APPLICANT(S)

Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C.
P.O. Box 398
Austin, TX 78767-0398
Phone: (512) 853-8800

Date: 3/28/07